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СУЧАСНІ НАПРЯМИ РОЗВИТКУ ТА ОСОБЛИВОСТІ АРХІТЕКТУРИ КОМП'ЮТЕРІВ

У статті розглянуто сучасні напрями розвитку та особливості архітектури комп'ютерів. Дане дослідження присвячене аналізу питань щодо організації та функціонування сучасних комп'ютерів та їх основних складових частин. Розглянуті основні компоненти та проаналізовані складові структури і функціонування сучасних комп'ютерів фон-нейманівського типу. Проаналізована структура пам'яті комп'ютера, та вивчена організаціята процедура взаємодії між її рівнями, зокрема розглянуто особливості сегментної організації пам'яті та проблеми і шляхи їх іиріщення щодо забезпечення захисту. Обгрунтовано головні принципи організації шин комп'ютера, операційних пристроїв та інших систем функціонування. Досліджено провідні тенденції в архітектурі сучасних процесорів, встановлено принципи побудови і архітектурні особливості паралельних комп'ютерних систем, запропоновано нові підходи щодо вивчення архітектури комп'ютерів і особливості їх побудови. Запропоновано та вдосконалено понятійний апарат щодо нейрокомп'ютерів та визначено їх архітектурні особливості. Обгрунтовано, що сучасні комп'ютерні архітектури базуються на принципах архітектури фон Неймана, що дозвряє встановити спільне зберігання команд і даних в одному адресному просторі пам'яті. Проаналізовано визначні структурні компоненти длсліджувної системи, що необхідними для ефективного функціонування та виконання поставлених завдань. Досліджено особливості функціонування компонентів сучасної архітектури та визначено головні вимоги до неї. Обгрунтовано необхідність та доцільність вимог, визначених специфікою функціонування інформаційних систем, що забезпечують високу швидкість, надійність та універсальність використання. Обгрунтовано вимоги до роботи високопродуктивних технічних засобів, що розглядаються за критерієм відповідності продуктивності та витрат ресурсів можна вважати метод їх дослідження та розробки нових логічних систем організації діяльності та продуктивності, а також удосконалення існуючих принципів організації машинних обчислень. Встановлено, що найбільш дієвим способом підвищення функціонування, розглядаючи цю проблему через призму зазначених особливостей, є паралельна обробка дій, опосередкована одночасним виконанням програм одночасно або їх компонентів, що складають, процедур, підпрограм, на незалежних пристроях. Удосконалено структуру модулярного нанокомп'ютера, що забезпечує виконання заданих операцій, реалізує ряд переваг багатозадачності. Доведено шляхи посилення функціональних можливостей нанокомп'ютера, призначеного для подання та обробки як дійсних, так і комплексних вхідних даних, а також при обробці їх у кільці цілих чисел, визначаються нейромережевими алгоритмами.

Ключові слова: *архітектура комп'ютерів, нейрокомп'ютер, нанокомп'ютер, процесор, пам'ять*

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CURRENT DIRECTIONS OF DEVELOPMENT AND FEATURES OF COMPUTER ARCHITECTURE

The article considers modern directions of development and features of the architecture of neurocomputers. This study is devoted to the analysis of issues related to the organization and functioning of modern computers and their main components. The main components are considered and the components of the structure and functioning of modern computers of the von Neumann type are analyzed. The structure of computer memory is analyzed, and the organization and procedure of interaction between its levels are studied, in particular, the features of segmental organization of memory and problems and ways to solve them regarding ensuring protection are considered. The main principles of organization of computer buses, operating devices and other functioning systems are substantiated. The leading trends in the architecture of modern processors have been investigated, the principles of construction and architectural features of parallel computer systems have been established, new approaches to the study of computer architecture and the features of their construction have been proposed. The conceptual apparatus for neurocomputers has been proposed and improved, and their architectural features have been determined. It is substantiated that modern computer architectures are based on the principles of the von Neumann architecture, which allows for the joint storage of commands and data in a single address space of memory. The significant structural components of the research system, which are necessary for the effective functioning and fulfillment of the tasks, are analyzed. The peculiarities of the functioning of components of modern architecture are investigated and the main requirements for it are determined. The necessity and feasibility of the requirements determined by the specifics of the functioning of information systems, which ensure high speed, reliability and universality of use, are substantiated. The requirements for the operation of high-performance technical means, considered according to the criterion of compliance with productivity and resource consumption, can be considered a method of their research and development of new logical systems for organizing activities and productivity, as well as improving existing principles of organizing computer calculations. It has been

established that the most effective way to improve functioning, considering this problem through the prism of the above-mentioned features, is parallel processing of actions, mediated by the simultaneous execution of programs or their constituent components, procedures, subroutines, on independent devices. The structure of a modular nanocomputer has been improved, ensuring the execution of specified operations and realizing a number of advantages of multitasking. The ways of enhancing the functional capabilities of a nanocomputer designed to represent and process both real and complex input data, as well as when processing them in a ring of integers, are determined by neural network algorithms.

Key words: *computer architecture, neurocomputer, nanocomputer, processor, memory*

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Introduction

For a long time, computer technology followed the path of massive parallelism, which is asSFCiated with the creation of multiprocessor computing systems, which are characterized by an increase in processing speed by combining several processors built according to the von Neumann architecture adopted as a model. Attention was also paid to the method of transitioning to a neural network logical basis, which provided for effective parallel processing at the algorithmic level and an increase in the level of process organization from an algorithmic point of view. Considering that neurocomputers are constantly in the field of view of modern scientists in various fields of science and technology, it can be argued that their relevance, namely their application, does not raise questions in the scientific community. Computers are usually classified according to various criteria, marked by their performance, portability, purpose, and other features. Our attention was focused on certain subgroups of them, namely neurocomputers and nanocomputers. Nanoelectronics aims to revolutionize modern information technology, where lithography using special chips can be argued. The challenge is to create small-sized equipment without losing functionality.

Analysis of recent research and publications

Research into current issues requires an analysis of the components of a set of recommendations for optimizing the design, development, and implementation of computer architecture components, based on future forecasts of their use. The large number of publications by scientists on the methodology of the chosen environment cannot be fully covered due to the relative novelty of the issues of analyzing the development of nanocomputer architectures. Yingjie W., Paul P., Jennings A. examine the methodology and main stages of Nanocomputer development and changes in their Architecture [1,2]. Doug G. consider the evolution of nanotechnologies and the specifics of their architecture [3]. Tyshchenko D., Franchuk T., Stepashkina K., Karpunin I., Desiatko A. examine general aspects of computer architecture [4,5]. Michael S., Montemerlo J., Christopher J., Opiteck D., Goldhaber G. analyze technologies and designs for electronic nanocomputers [6]. In the article Tyshchenko D., Franchuk T., Zakharov R., Moskalenko V., the support of dynamic security needs using VPN tools is investigated [7]. The work of Kapiton A., Franchuk T., Tyshchenko D., Desyatko A., Zakharov R. is devoted to the analysis of requirements for modern processors for the secure operation of information systems and networks [8]. Durbeck L., Nicholas M. study the main aspects of the honeycomb matrix: architecture for nanocomputing [9]. Beckett B., Jennings A. analyze the current state and prospects for the development and modification of nanocomputer architecture [10]. Kolesnytskyi O. will explore the basic principles of building the architecture of spike neurocomputers[11]. Vovk B. issues of organization and functioning of modern computers and their main components[12]. Scientific institutions in our country and leading countries of the world conduct research that includes methods of non-iterative training of neural networks[13]. The main advantages of modern nanocomputers, computer architectures for nanotechnologies considered on the way to nanocomputing, as well as the ranking of the best models of the past year are presented in numerous publications [14]. Analysis of processors included in the rating of the best models in recent years according to various criteria and research into the problem of choosing the optimal processor to meet the need for ensuring information security in the network, advice and recommendations for their selection for the security of information systems and networks are presented in numerous studies. Analysis of the development directions and features of the architecture of neurocomputers has allowed us to identify those gaps in the field of study that need to be closed. A number of issues regarding the organization and functioning of modern computers and their main components require further analysis. The studied main components and components of the structure and functioning of modern von Neumann-type computers require a more thorough analysis, and therefore there is no doubt about the relevance of a comprehensive study of this issue [14].

Main part

Modern computer architectures are based on the principles of the von Neumann architecture, which involves a central processing unit, memory, and peripheral devices that interact with each other. The main requirements for modern architecture include high processor (CPU) performance, speed and amount of random access memory (RAM), data storage speed (SSD/HDD), graphics processing unit (GPU) power, as well as the availability of efficient interfaces and ports for connecting various devices. Key components and requirements are presented in the figure 1.

KEY COMPONENTS AND REQUIREMENTS	
Central Processing Unit (CPU)	Executes instructions and calculations.
Memory	Contains both programs and data that are processed by the processor.
Input/Output Devices	llow interaction with the user and the outside world.
Data and Address Bus	Provide communication and information transfer between all components.

Fig. 1. Key components and requirements table

The key requirements for modern architecture are briefly presented in Figure 2. These requirements shape modern computer systems that provide high speed, reliability, and versatility of use.

KEY REQUIREMENTS FOR MODERN ARCHITECTURE	
High CPU performance	Speed of task execution
RAM speed and capacity	Important for program operation and multitasking
Storage speed (SSD/HDD)	Affects system and program boot times
GPU power	Required for graphics processing, especially in visualization-intensive applications.
Efficient interfaces and ports	Allows you to connect various devices (e.g. USB, HDMI)

Fig. 2. The key requirements for modern architecture's table

It can be argued that the most effective way to improve functioning, considering this problem through the prism of the above features, is parallel processing of actions, mediated by the simultaneous execution of programs or their constituent components, procedures, subroutines, on independent devices. It can be argued that the most effective way to improve functioning, considering this problem through the prism of the above features, is parallel processing of actions, mediated by the simultaneous execution of programs or their constituent components, procedures, subroutines, on independent devices. The basis of the active development of neurocomputers is the fundamental difference between neural network algorithms for solving problems from single-processor, small-processor, and transcomputer algorithms. The disadvantage of the predecessors is the low productivity due to the sequential nature of the organization of the computing process. The presence of one processor determines the low efficiency of memory usage. Predecessors and neurocomputers also differ in the principle of interaction between the structure of the machine and the task to be solved. For single-processor machines, with their "rigid" structure, the developer has to adjust the algorithm for solving the problem to the structure of the machine[1-3].

When using neurocomputers, the developer adjusts the structure of the machine to the problem being solved. A neurocomputer (NC) is a computing system with a hardware and software architecture adequate to the execution of algorithms presented in a neural network logic base. The main problems of NC creation are the development of super-parallel neural network algorithms for formalizable problems and their parallelization in accordance with the architecture of the switching system, as well as the development of new methods for solving informal problems. The application of the system of final classes (SFC) provides independent and parallel processing of each digit of the number identified with neurons, which determines the structure of the NC, the central processor of which is built on the basis of neural networks of the finite ring (NNFR). Taking into account the low-digit number, a non-positional NC can be completed in the form of a set of tables for the implementation of a number of basic modular operations. Coding in SFC and the use of neural networks (NN) allows parallel computing algorithms at the level of elementary operations. The following properties of residues are obvious from the algorithm for constructing the SFC code: independence, equality, and sparseness. The NC functioning in the SFC, or the "modular NN" can be completed in the form of separate tracts based on the number of bases, working independently in time, which can be designed as elementary pro-cessors, implemented in the form of NNFR, that is, the structure of the non-positional NN has a modular neural organization for information processing, transmission and storage. One of the approaches to the solution of the problem of increasing the reliability of the NC operating in the SFC is based on the redistribution of its channels when part of the working or control channels fail[5-8,11-13].

At the same time, under the reliability of the NC, it still has the property of maintaining operability in the event of channel failures, possibly with a decrease in the permissible limits of some indicators of the quality of functioning. Я the core of a fault-tolerant NC is a central processor consisting of n-parallel elementary processors (EP), where n is the number of SFC modules. Taking into account the modularity of the NN structure functioning in the SFC, the central processor can be expanded by various groups of NN models. NN models are determined by neuron models and the

structure of network connections. The central processor consists of a modular arithmetic device that performs modular operations, a non-modular arithmetic device that performs non-modular procedures, and a control device. The arithmetic device performs calculations and can be performed in the form of separate working in parallel. The need to perform operations of a non-positional type, associated with actions on the whole number, requires the inclusion of a processor, non-modular, consisting of a block of positional characteristics, which has a buffer memory, and a control block, implemented on the basis of formable, general and combined NNs of complex input data, as well as when processing them in a ring of wholes or villages, are determined by neural network algorithms of SFC arithmetic[9-10].

Some of them perform calculations, and some of them form an output signal in accordance with their topology and the values of the coefficients of interneuron connections. Let's list the functions of the positional characteristics and control blocks: determining the sign of a number, comparing numbers, dividing, rounding, determining overflow, expanding the base system, determining the positional characteristics of a number, and detecting errors. The execution of these functions is necessary to determine the arrangement of numbers in a numerical range. The block of positional characteristics includes a scheme for converting numbers from SFC to the generalized positional numbering system (PNS). To restore the number in SFC, a conversion scheme is used. Some positional characteristics, such as the sign of the number or the number of the interval in which the number is located, use the values of the most significant digit of the number represented in the PNS. This follows from the one-to-one correspondence between the numbers presented in SFC and PNS. Therefore, the scheme for determining the sign of a number is included in the block of positional characteristics. An error in the code combination and the determination of overflow of the bit grid of the processor is also determined by the value of the highest bit. This function is performed by the error detection and correction scheme. To expand the basic system, the basic expansion scheme is included in the composition. The functions of division, base reduction, number rounding, and scaling are performed by the scheme of modular execution of non-modular operations. To implement the operation of comparing numbers or determining the intervals in which they are located, knowledge of all the digits of numbers represented in PNS is required. The functions of division, base reduction, number rounding, and scaling are performed by the scheme of modular execution of non-modular operations. To implement the operation of comparing numbers or determining the intervals in which they are located, knowledge of all the digits of numbers represented in PNS is required. . This function is performed by the number comparison scheme included in the positional characteristics block. The positional characteristic of the rank and the core of the number is determined by the scheme for determining the rank of the number based on the values of the digits of the numbers presented in the SFC, and is used to determine and correct errors, expand the base system, rounding, division, and a number of other operations. With the help of the rank and kernel of a number, non-modular operations are relatively easily implemented. The rank and kernel can be calculated using modular operations. The training and reconfiguration block provides training of neural networks to solve a specific task and configures the processor when a part of the working or control channels fails. A necessary element of a non-positional processor, as well as a positional one, is a processor memory device consisting of a random access memory device and a non-volatile memory device; a non-volatile memory device is intended for storing commands and data, а постоянного запоминающего устройство нужно для программ изменения коэффициентов connections between neurons and some numerical constants. The control device provides storage of microprograms for all operations and organizes the operation of the entire processor by sending control signals to the control units of the main devices. The control device indicated on the structural diagram is intended for general synchronization of NC work, organization of the training process, and loading of weight coefficients into each block. This control device is not directly related to the standard interface controller and has a specific set of commands. For input and output of information, an input-output device consisting of input-output buffer memory and number conversion blocks is included in the structure of the non-positional processor.

Today, humanity strives for optimization, comfort and simplification. These urges push us to review everything that surrounds us, notice the shortcomings and bottlenecks and automate them, make them better. Such disadvantages often include the inconvenient shape of the device or its size. Thus, it is necessary to reduce the size of the computer, make its display thin and at the same time not lose its efficiency. The project to create nanocomputers is mostly not focused on this segment and already involves the creation of government programs in Japan, the USA and the EU, as well as in fifty other countries. Nanoelectronics will not only change the current information technologies, but also create an opportunity to reduce the minimum allowable computer sizes to the subcellular level. Nanoscopic lithography, which is essentially a descendant of the small-scale lithography used today for the production of computer chips, is advanced in the technology of creating nanostructures. There are clear problems and great opportunities behind the driver system of such computers. As for the computer as such, there is currently no nanoversion of the ego, because creating a computer of such small sizes and at the same time not losing its functionality is an extremely difficult task. It requires huge human efforts and huge material investment. However, albeit slowly, work on the design and creation of this device is already actively underway. So far, only nanotransistors for a nanocomputer have been successfully developed, but, without a doubt, this is a significant step for mankind towards the creation of the "computer of the future".

Conclusions

The architecture of a nanocomputer is based on the use of nanotechnology to create devices at the molecular or atomic level. Unlike traditional computers, nanocomputers work with nanoparticles and use nanotransistors as the basis for nanoprocessors. The specific architecture of a nanocomputer can vary significantly depending on the field of application and the materials used, but its key feature is the creation of computing elements and circuits using matter at the nanolevel. Based on the statement that the architecture of a nanocomputer is based on the use of nanotechnology to

create devices at the molecular or atomic level, it can be argued that unlike traditional computers, nanocomputers work with nanoparticles and use nanotransistors as the basis for nanoprocessors. The specific architecture of a nanocomputer can vary significantly depending on the field of application and the materials used, but its key feature is the creation of computing elements and circuits using matter at the nanolevel. The structure of the modular NC not only ensures the performance of the required operations, but also realizes the main advantage of the final class system – the parallelism of the operations. All this makes it possible to realize completely parallel access to almost all nodes of the NC and makes it possible to develop a NC, free from the shortcomings of the classical structure of the technical device. Thus, a fault-tolerant structure of a high-performance NC based on the use of SFC is proposed. The combination of such properties as the independence of arithmetic operations and massive parallelism of data processing allows the use of the structure of modular neural networks for data processing. The functional possibilities of NC intended for presentation and processing currently require further research.

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